AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently amended): A memory system comprising:

a plurality of memory modules provided with memory areas for holding data and buffer sections for sending and receiving the data;

a hard disk device to which the data stored in said memory modules is copied at predetermined time periods;

a control device which, when an arbitrary memory module is being replaced and is not capable of transmitting data to other memory modules of a ring bus of which it is a part, switches an operational mode of ~~a~~ the ring bus from a unidirectional bus which either sends or receives a signal unidirectionally, to a bi-directional bus which sends and receives a signal bi-directionally, detects an address space of said memory module to be replaced, and accesses a memory area in said hard disk device corresponding to the detected address space at the time when an access to said memory module being replaced is requested; and

a CPU which controls said control device for access operation to said memory modules,

wherein said buffer sections are connected in series to form the ring bus with said control device, each having a buffer circuit for causing said ring bus to operate as said unidirectional bus or said bi-directional bus in accordance with an instruction from said control device,

whereby signals from each remaining memory module can be transmitted to any other remaining memory module without loss of data by reason of a memory module being replaced and not capable of transmitting data.

2. (Currently amended): A memory system comprising:

a plurality of memory modules provided with memory areas for holding data and buffer sections for sending and receiving the data;

a hard disk device to which the data stored in said memory modules is copied at predetermined time periods;

a storage to which data stored in an arbitrary memory module is temporarily copied;

a control device which, when an arbitrary memory module is being replaced and is not capable of transmitting data to other memory modules of a ring bus of which it is a part, switches an operational mode of ~~a~~ the ring bus from a unidirectional bus which either sends or receives a signal unidirectionally, to a bi-directional bus which sends and receives a signal bi-directionally, detects an address space of said memory module to be replaced, copies data corresponding to the detected address space from said hard disk device to said storage, and accesses a memory area in said storage corresponding to the detected address space at the time when an access to said memory module being replaced is requested; and

a CPU which controls said control device for access operation to said memory modules,

wherein said buffer sections are connected in series to form the ring bus with said control device, each having a buffer circuit for causing said ring bus to operate as said unidirectional bus or said bi-directional bus in accordance with an instruction from said control device,

whereby signals from each remaining memory module can be transmitted to any other remaining memory module without loss of data by reason of a memory module being replaced and not capable of transmitting data.

3. (Original): The memory system according to claim 1, further comprising a short-circuit device for, when an arbitrary memory module is replaced, recovering bus connection which is disconnected by removing said memory module.

4. (Original): The memory system according to claim 2, further comprising a short-circuit device for, when an arbitrary memory module is replaced, recovering bus connection which is disconnected by removing said memory module.

5. (Currently amended): A memory system comprising:

a plurality of memory modules provided with memory areas for holding data and buffer sections for sending and receiving the data;

a hard disk device to which the data stored in said memory modules is copied at predetermined time periods;

a storage to which data stored in an arbitrary memory module is temporarily copied;

a short-circuit device which, when an arbitrary memory module is being replaced, recovers a bus connection which is disconnected by removing said memory module being replaced;

a control device which, when an arbitrary memory module is being replaced and is not capable of transmitting data to other memory modules of a ring bus of which it is a part, detects an address space of said memory module being replaced, copies data corresponding to the detected address space from said hard disk device to said storage, and accesses a memory area in said storage corresponding to the detected address space at the time when an access to said memory module being replaced is requested; and

a CPU which controls said control device for access operation to said memory modules,

wherein said buffer sections are connected in series to form a unidirectional bus which either sends or receives a signal unidirectionally,

whereby signals from each remaining memory module can be transmitted to any other remaining memory module without loss of data by reason of a memory module being replaced and not capable of transmitting data.

6. (Original): The memory system according to claim 3, wherein said short-circuit device is a dummy module which is inserted instead of said memory module to be replaced and is provided with a short-circuit line for short-circuiting bus connection which is disconnected by removing said memory module.

7. (Original): The memory system according to claim 4, wherein said short-circuit device is a dummy module which is inserted instead of said memory module to be replaced and is provided with a short-circuit line for short-circuiting bus connection which is disconnected by removing said memory module.

8. (Original): The memory system according to claim 5, wherein said short-circuit device is a dummy module which is inserted instead of said memory module to be replaced and is provided with a short-circuit line for short-circuiting bus connection which is disconnected by removing said memory module.

9. (Original): The memory system according to claim 3, wherein said short-circuit device is an FET switch, which is provided in association with said memory modules,

respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module, and

in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory module to be replaced and turning OFF the FET switches provided in association with the other memory modules.

10. (Original): The memory system according to claim 4, wherein said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module, and

in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory module to be replaced and turning OFF the FET switches provided in association with the other memory modules.

11. (Original): The memory system according to claim 5, wherein said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module, and

in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory module to be replaced and turning OFF the FET switches provided in association with the other memory modules.

12. (Previously presented): The memory system according to claim 3, wherein said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with shorting pins which short-circuits bus connection, which is disconnected by removing said memory module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted.

13. (Previously presented): The memory system according to claim 4, wherein said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with shorting pins which short-circuits bus connection, which is disconnected by removing said memory module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted.

14. (Previously presented): The memory system according to claim 5, wherein said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with shorting pins which short-circuits bus connection, which is disconnected by removing said memory module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted.

15. (Previously presented): The memory system according to claim 2, wherein said storage is a memory module for mirroring which is provided with a memory area for holding data and a buffer section for sending and receiving data.

16. (Previously presented): The memory system according to claim 5, wherein said storage is a memory module for mirroring which is provided with a memory area for holding data and a buffer section for sending and receiving data.

17. (Original): The memory system according to claim 2, wherein said storage is a memory for graphics.

18. (Original): The memory system according to claim 5, wherein said storage is a memory for graphics.

19. (Original): The memory system according to claim 2, wherein said storage is free memory areas of the other memory modules excluding said memory module to be replaced.

20. (Original): The memory system according to claim 5, wherein said storage is free memory areas of the other memory modules excluding said memory module to be replaced.

21-43. **Canceled**.

44. (Previously presented): The memory system according to claim 1, wherein said control device comprises:

a first buffer circuit for receiving a signal from a first input/output connection to the ring bus;

a second buffer circuit for sending a signal to the first input/output connection to the ring bus;

a third buffer circuit for receiving a signal from a second input/output connection to the ring bus; and

a fourth buffer circuit for sending a signal to the second input/output connection to the ring bus.

45. (Previously presented): The memory system according to claim 2, wherein said control device comprises:

a first buffer circuit for receiving a signal from a first input/output connection to the ring bus;

a second buffer circuit for sending a signal to the first input/output connection to the ring bus;

a third buffer circuit for receiving a signal from a second input/output connection to the ring bus; and

a fourth buffer circuit for sending a signal to the second input/output connection to the ring bus.

46. (Previously presented): The memory system according to claim 5, wherein said control device comprises:

a first buffer circuit for receiving a signal from a first input/output connection to the ring bus;

a second buffer circuit for sending a signal to the first input/output connection to the ring bus;

a third buffer circuit for receiving a signal from a second input/output connection to the ring bus; and

a fourth buffer circuit for sending a signal to the second input/output connection to the ring bus.